**MODULE DESCRIPTION FORM**

**نموذج وصف المادة الدراسية**

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| **Module Information****معلومات المادة الدراسية** |
| **Module Title** | Fundamentals of Electrical Engineering (DC) | **Module Delivery** |
| **Module Type** | Core | * **☒ Theory**
* **☐ Lecture**
* **☒ Lab**
* **☒ Tutorial**
* **☐ Practical**
* **☐ Seminar**
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| **Module Code** | MIET1101 |
| **ECTS Credits** | 6 |
| **SWL (hr/sem)** | 150 |
| **Module Level** | UGI | **Semester of Delivery** | 1 |
| **Administering Department** | MIET | **College** | Al Hikma University College |
| **Module Leader** | Ayman Khalil Ibrahim | **e-mail** |  |
| **Module Leader’s Acad. Title** |  | **Module Leader’s Qualification** | Ph.D. |
| **Module Tutor** | Farah Mazin Salim | **e-mail** | Farah.mazin@hiuc.edu.iq |
| **Peer Reviewer Name** | Jameel Kahdum Abid | **e-mail** | jameel.kadhim@hiuc.edu.iq |
| **Scientific Committee Approval Date** | 11/11/2023 | **Version Number** | 1.0 |

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| **Relation with other Modules****العلاقة مع المواد الدراسية الأخرى** |
| **Prerequisite module** | None | **Semester** |  |
| **Co-requisites module** | None | **Semester** |  |

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| **Module Aims, Learning Outcomes and Indicative Contents****أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية** |
| **Module Objectives****أهداف المادة الدراسية** | 1.To develop knowledge on standard units of electricity and understanding of DC circuit theorems.2.To understand voltage, current and power of DC circuits.3.To learn the basic concept of DC electrical circuits connections.4.To explain the DC electrical circuits.5.To understand basic laws of electricity.6.To perform DC-network theorem.7.To perform DC-circuit analysis methods.8.To understand independent sources and dependent sources. |
| **Module Learning Outcomes****مخرجات التعلم للمادة الدراسية** | 1.Recognize how electricity works in electrical circuits.2.List the various terms associated with electrical circuits.3.Summarize what is meant by a basic electric circuit.4.Describe electrical power, voltage, and current.5.Define Ohm's law and define the relation between voltage, resistance, and current.6.Identify the basic circuit elements and their applications.7.Discuss the operations of power and energy in electric circuit.8.Discuss the various properties of resistors connections.9.Explain the two Kirchhoff’s laws used in circuit analysis.10.Identify the implementation of resistor circuit’s connection.11.Learn measurements of voltage ad current.12.Practical Identification of resistance based on color code. |
| **Indicative Contents****المحتويات الإرشادية** | Indicative content includes the following.DC circuits – Current and voltage definitions, and circuit elements, Combining resistive elements in series and parallel. Kirchhoff’s laws and Ohm’s law, Network reduction, Introduction to mesh and nodal analysis. [20 hrs.]Conversion of delta – connected resistance into an equivalent Wye connection & Vic versa. [10 hrs.]Fundamentals of the Power sources connected in parallel, Thevenin and Norton equivalent circuits, current and voltage division, Loop current method, Super position method, maximum power transfer, Non- linear direct current circuit [20 hrs.]Independent sources and dependent sources [10 hrs.]source transformation [5 hrs.]Revision problem classes [5 hrs.] |

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| **Learning and Teaching Strategies****استراتيجيات التعلم والتعليم** |
| **Strategies** | The main strategy that will be adopted in delivering this module is to encourage students’ participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials, and by considering types of simple experiments involving some sampling activities that are interesting to the students. |

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| **Student Workload (SWL)****الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا** |
| **Structured SWL (h/sem)****الحمل الدراسي المنتظم للطالب خلال الفصل** | 79 | **Structured SWL (h/w)****الحمل الدراسي المنتظم للطالب أسبوعيا** | 5 |
| **Unstructured SWL (h/sem)****الحمل الدراسي غير المنتظم للطالب خلال الفصل** | 71 | **Unstructured SWL (h/w)****الحمل الدراسي غير المنتظم للطالب أسبوعيا** | 5 |
| **Total SWL (h/sem)****الحمل الدراسي الكلي للطالب خلال الفصل** | **150** |

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| **Module Evaluation****تقييم المادة الدراسية** |
| **As** | **Time/Number** | **Weight (Marks)** | **Week Due** | **Relevant Learning Outcome** |
| **Formative Assessment** | **Quizzes** | 2 | 10% (10) | 5, 10 | LO #1, #2 and #10, #11 |
| **Online Assignments** | 2 | 10% (10) | 2,12 | LO #3, #4 and #6, #7 |
| **Projects**  | 1 | 6% (6) | Continuous | LO# 1-12 |
| **Lab** | 10 | 10% (10) | Continuous | LO# 1-12 |
| **Report** | 1 | 4% (4) | 13 | LO # 5, 8, 9, 12 |
| **Summative Assessment** | **Midterm Exam** | 3hr | 10% (10) | 7 | LO #1 - #7 |
| **Final Exam** | 4hr | 50% (50) | 16 | All |
| **Total assessment** | 100% (100 Marks) |  |  |

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| **Delivery Plan (Weekly Syllabus)****المنهاج الاسبوعي النظري** |
| **Week**  | **Material Covered** |
| **Week 1** | Symbols and abbreviations, Units, Electric circuits, and its elements. |
| **Week 2** | The direct–current network (Ohm’s law, Kirchhoff’s voltage and current laws & their use in network). |
| **Week 3****Week 4** | Series elements and Voltage DivisionParallel elements and Current Division |
| **Week 5** | Power sources are connected in parallel, |
| **Week 6** **Week 7** | Circuit analysis methods:1- Node voltage method.2- Loop current method. |
| **Week 8** | Mid-term exam |
| **Week 9** | Conversion of delta–connected resistance into an equivalent Wye connection & Vic versa |
| **Week 10-13** | Circuit analysis Theorems:1.Superposition2.Thevenin3.Norton4.Maximum power |
| **Week 14-15** | Independent sources and Dependent sources, source transformation and preparation for final exam |

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| **Delivery Plan (Weekly Lab. Syllabus)****المنهاج الاسبوعي للمختبر** |
| **Week**  | **Material Covered** |
| **Week 1** | Introduction to Electrical Elements, Sources, and Measuring Devices Related To Electrical Circuits. |
| **Week 2** | Resistance Measurement Based On AVO Meter Readings and Color Code Identification. |
| **Week 3** | Verification Of Ohm's Law |
| **Week 4-5** | Verification Of KVL And KCL |
| **Week 6-7** | Verification Of Thevenin’s and Norton’s Theorems |
| **Week 8-9** | Verification Of The Superposition Theorem |
| **Week 10** | Verification Of The Maximum Power Transfer Theorem |
| **Week 11** | Verification Of The Nodal Voltage Theorem |
| **Week 12** | Verification Of The Mesh Theorem |
| **Week 13-14** | Practical Implementation Of Independent Sources And Dependent Sources |
| **Week 15** | Preparation for Final Exam |

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| **Learning and Teaching Resources****مصادر التعلم والتدريس** |
|  | **Text** | **Available in the Library?** |
| **Required Texts** | Fundamentals of Electric Circuits, C.K. Alexander and M.N.O Sadiku, McGraw-Hill Education | Yes |
| **Recommended Texts** | Electric Circuits Seventh Editionوو Schaum’s Outline Series | No |
| **Websites** | https://www.youtube.com/watch?v=SfKw8bHk7-o (for practical implementation of Independent sources and Dependent sources, **Weeks 13-14**) |

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|  **Grading Scheme****مخطط الدرجات** |
| **Group** | **Grade** | **التقدير** | **Marks %** | **Definition** |
| **Success Group****(50 - 100)** | **A -** Excellent | **امتياز** | 90 - 100 | Outstanding Performance |
| **B -** Very Good | **جيد جدا**  | 80 - 89 | Above average with some errors |
| **C -** Good | **جيد** | 70 - 79 | Sound work with notable errors |
| **D -** Satisfactory | **متوسط**  | 60 - 69 | Fair but with major shortcomings |
| **E -** Sufficient | **مقبول**  | 50 - 59 | Work meets minimum criteria |
| **Fail Group****(0 – 49)** | **FX –** Fail | **راسب (قيد المعالجة)** | (45-49) | More work required but credit awarded |
| **F –** Fail | **راسب** | (0-44) | Considerable amount of work required |
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| **Note:** Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above. |